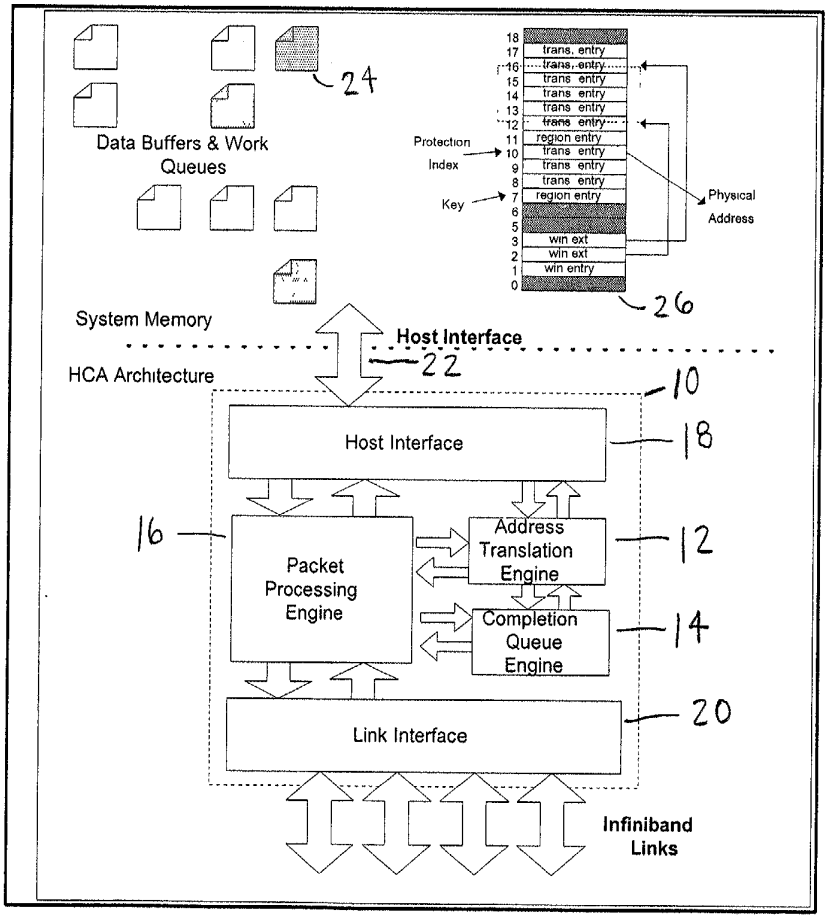

FIG. 1

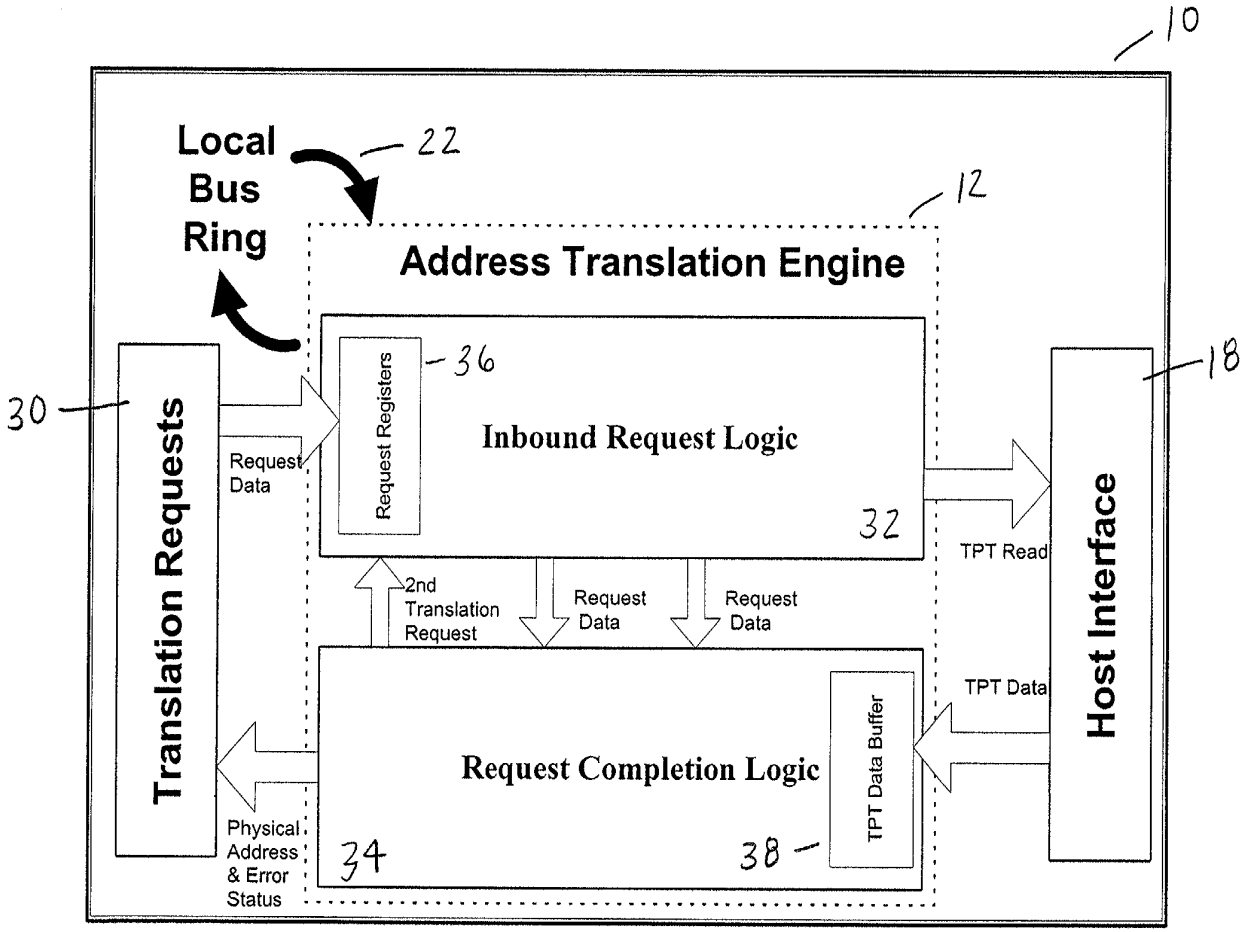
10
Local Bus Ring
22
12
Address Translation Engine
Request Registers
36
Inbound Request Logic
32
30
Translation Requests
Request Data
18
Host Interface
TPT Read
2nd Translation Request
Request Data
Request Data
TPT Data
TPT Data Buffer
Request Completion Logic
34
38
Physical Address & Error Status

FIG. 2

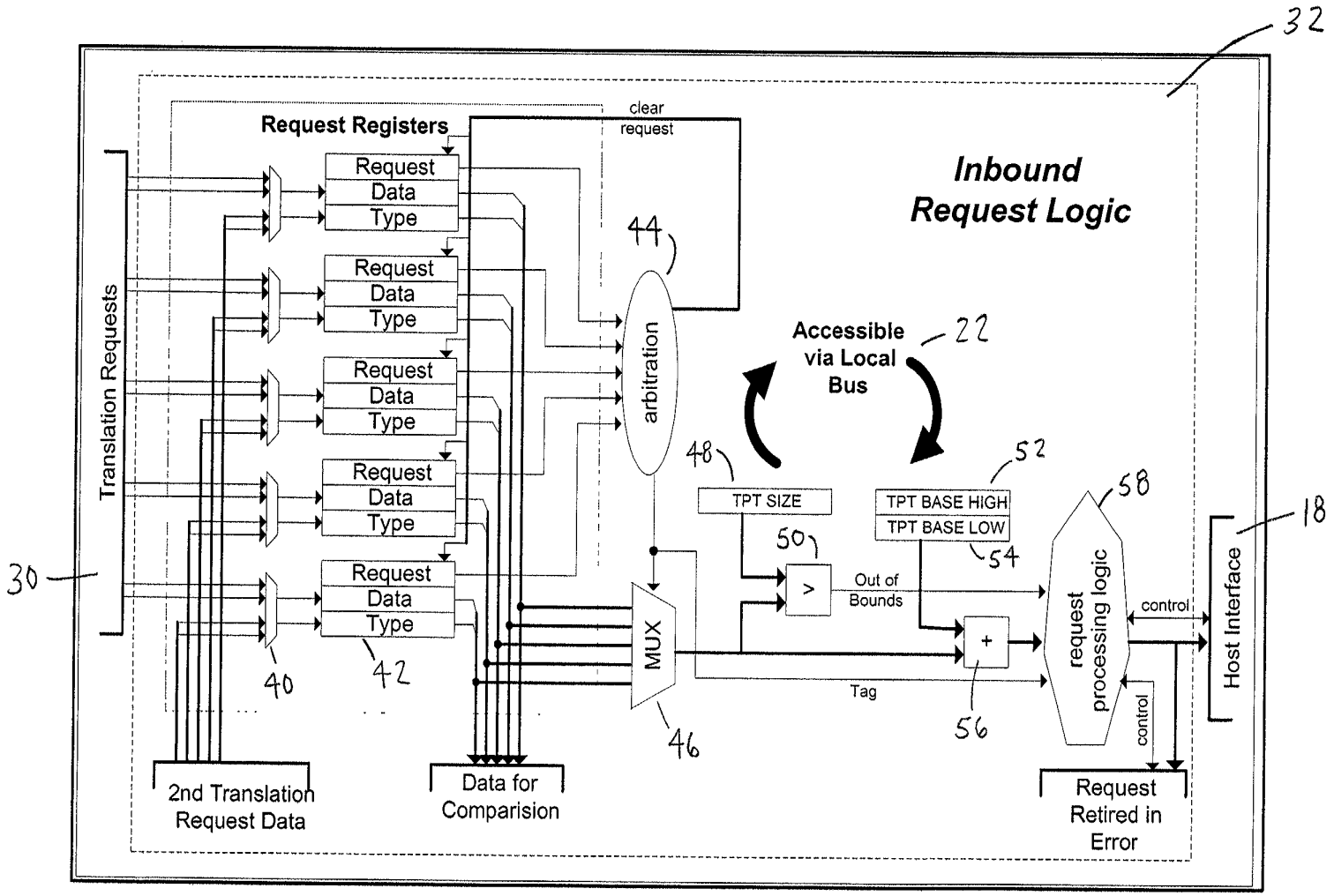
32
Request Registers
clear request
Request
Data
Type
Inbound Request Logic
44
arbitration
Translation Requests
Accessible via Local Bus
22
48
52
TPT SIZE
TPT BASE HIGH
TPT BASE LOW
58
50
54
>
Out of Bounds
request processing logic
control
18
Host Interface
30
MUX
+
Tag
40
42
46
56
control
2nd Translation Request Data
Data for Comparision
Request Retired in Error

FIG. 3

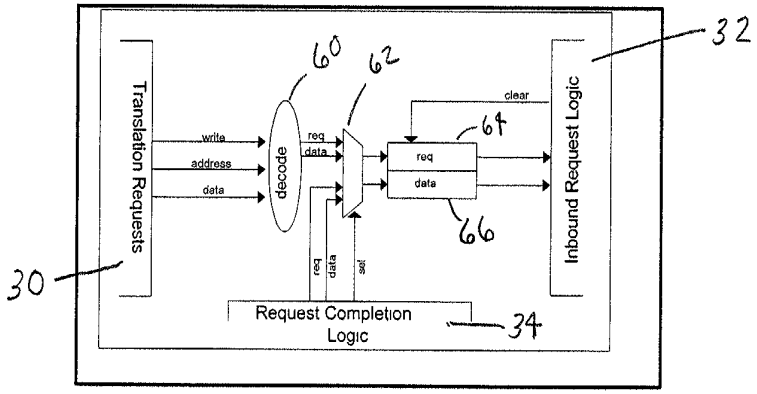
Translation Requests
30
write
address
data
decode
60
62
req
data
clear
64
req
data
66
Inbound Request Logic
32
req
data
sel
Request Completion Logic
34

FIG. 4

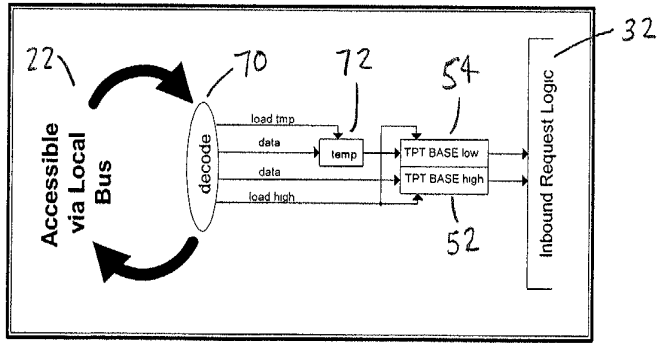
22
Accessible via Local Bus
70
72
54
load tmp
data
temp
data
load high
decode
TPT BASE low
TPT BASE high
52
Inbound Request Logic
32

FIG. 5

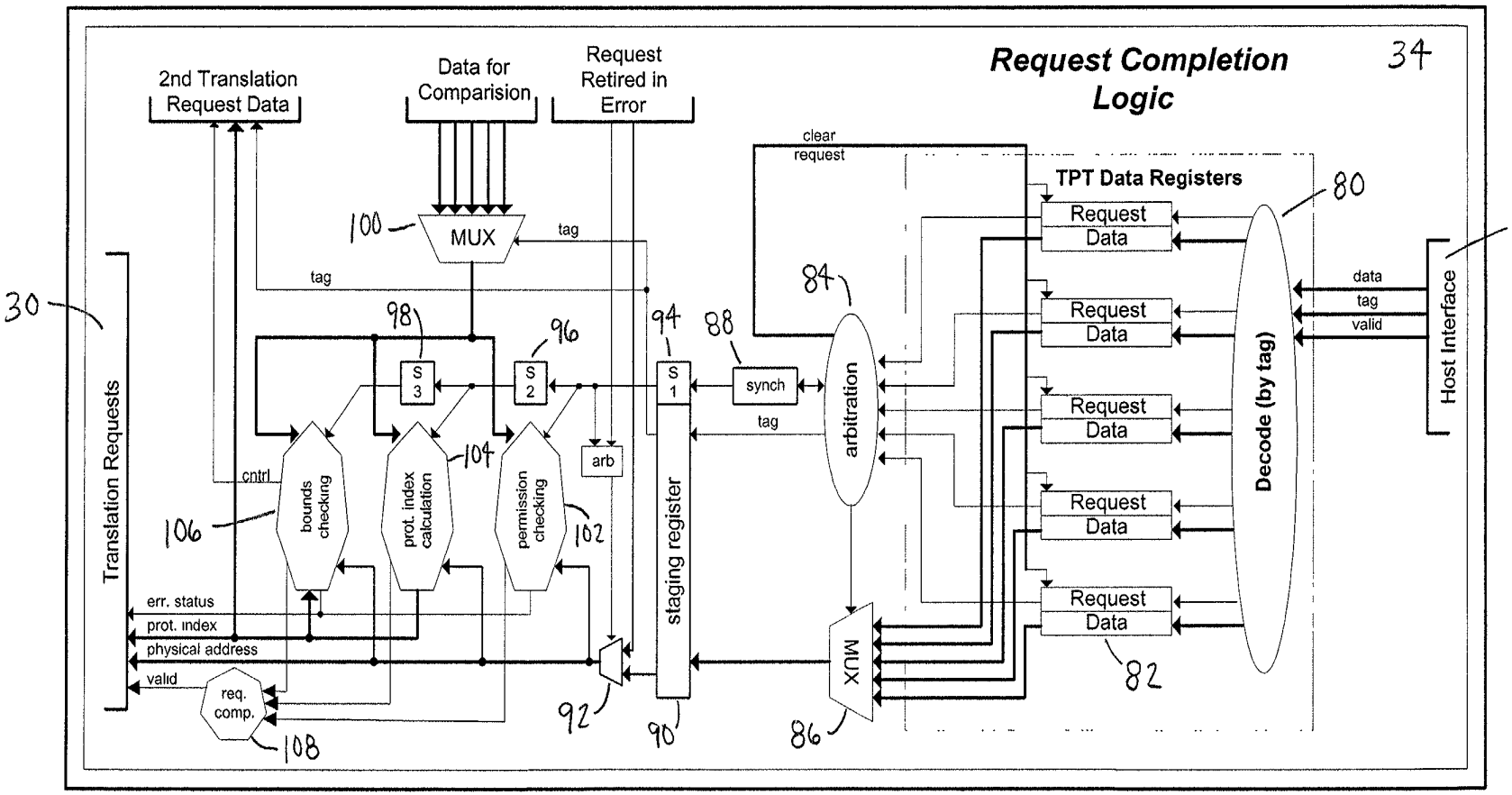
Request Completion Logic
34
2nd Translation Request Data
Data for Comparision
Request Retired in Error
clear request
TPT Data Registers
80
Request Data
Request Data
Request Data
Request Data
Request Data
82
data
tag
valid
Host Interface
18
30
Translation Requests
100
MUX
tag
tag
98
96
94
88
84
S 3
S 2
S 1
synch
arbitration
tag
cntrl
bounds checking
prot. index calculation
permission checking
104
106
102
arb
staging register
Decode (by tag)
err. status
prot. index
physical address
valid
req. comp.
108
92
90
86
MUX

FIG. 6

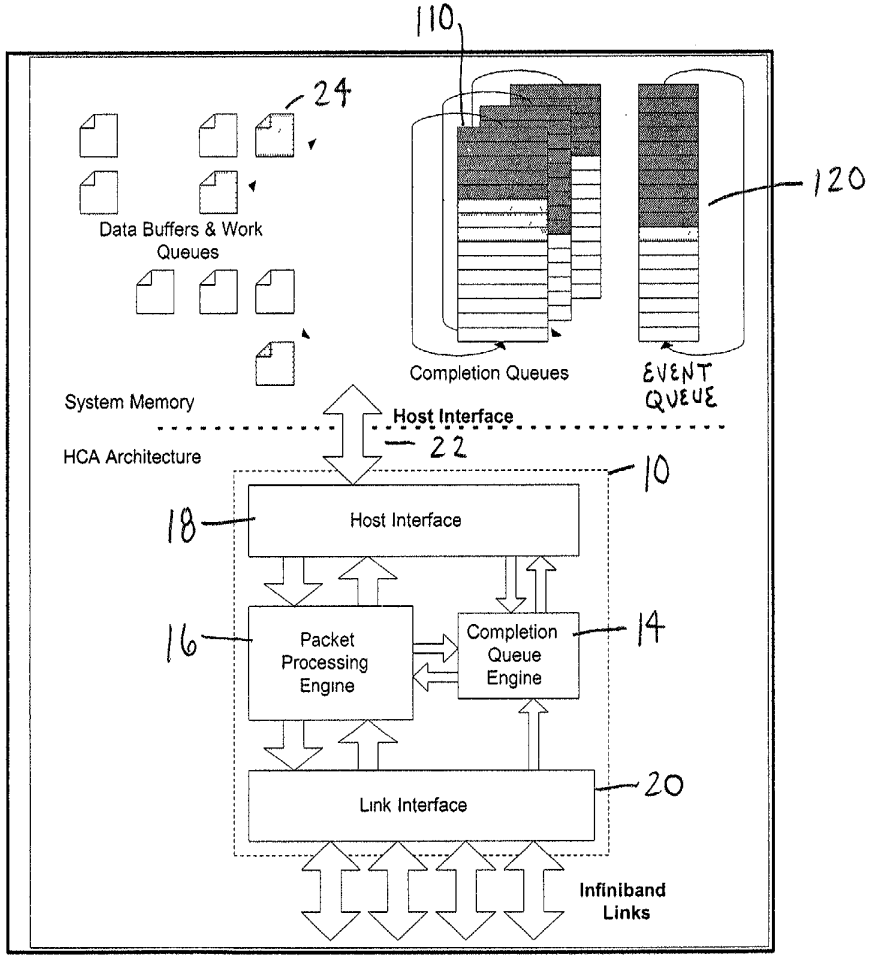
110
24
120
Data Buffers & Work Queues
Completion Queues
EVENT QUEUE
System Memory
Host Interface
22
HCA Architecture
10
18
Host Interface
16
Packet Processing Engine
Completion Queue Engine
14
Link Interface
20
Infiniband Links

FIG. 7

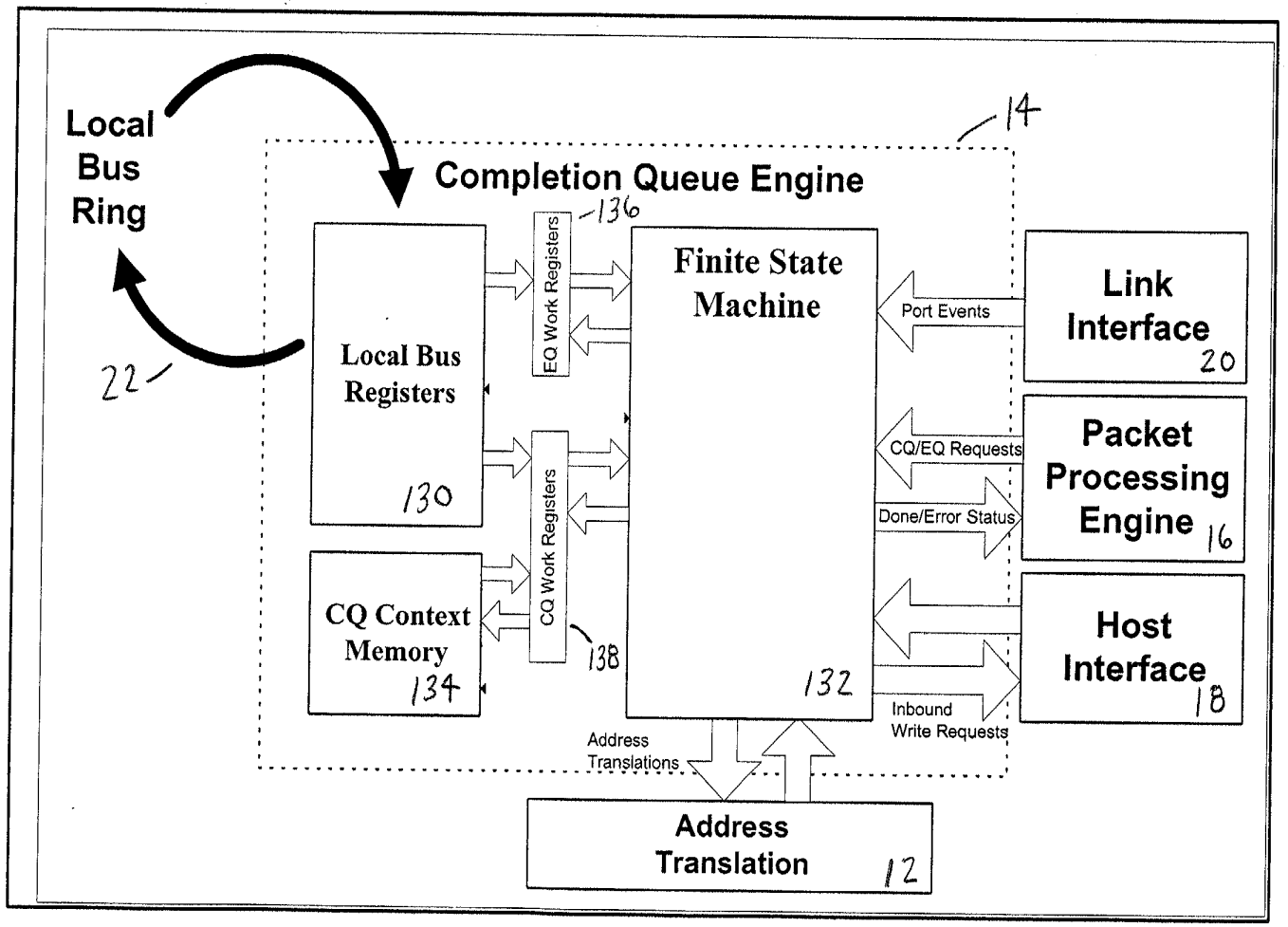
Local Bus Ring
14
Completion Queue Engine
136
EQ Work Registers
Finite State Machine
Link Interface 20
Port Events
Local Bus Registers 130
22
CQ/EQ Requests
Packet Processing Engine 16
Done/Error Status
CQ Work Registers
CQ Context Memory 134
138
132
Host Interface 18
Inbound Write Requests
Address Translations
Address Translation 12

FIG. 8

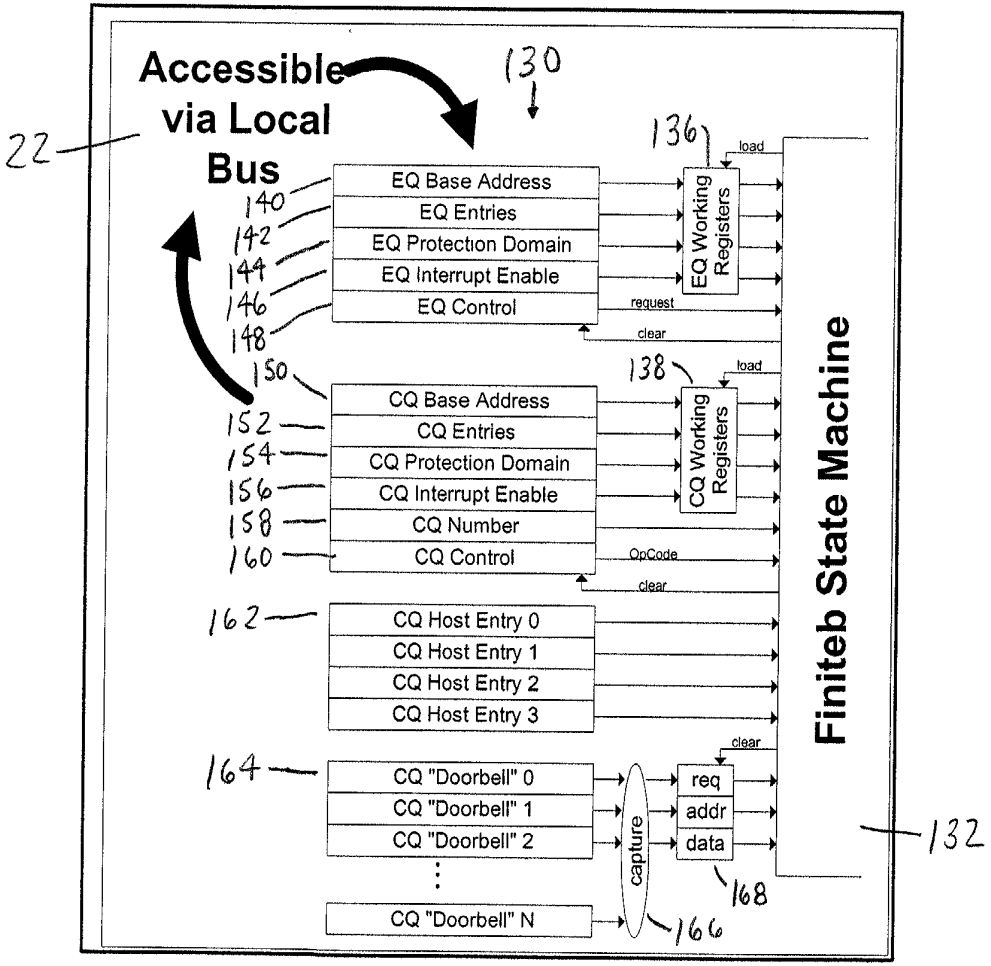
Accessible via Local Bus
22
130
136
load
EQ Base Address
EQ Entries
EQ Protection Domain
EQ Interrupt Enable
EQ Control
140
142
144
146
148
EQ Working Registers
request
clear
138
load
150
CQ Base Address
CQ Entries
CQ Protection Domain
CQ Interrupt Enable
CQ Number
CQ Control
152
154
156
158
160
CQ Working Registers
OpCode
clear
162
CQ Host Entry 0
CQ Host Entry 1
CQ Host Entry 2
CQ Host Entry 3
clear
164
CQ "Doorbell" 0
CQ "Doorbell" 1
CQ "Doorbell" 2
CQ "Doorbell" N
capture
req
addr
data
168
166
Finiteb State Machine
132

FIG. 9

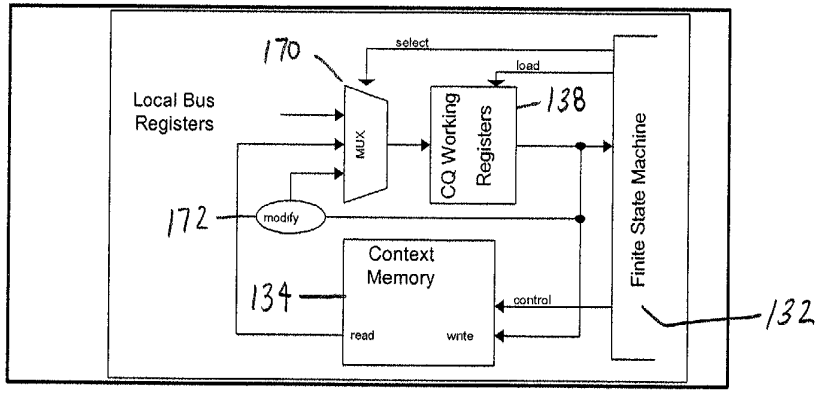

FIG. 10

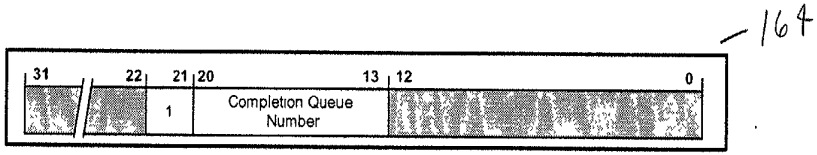

FIG. 11

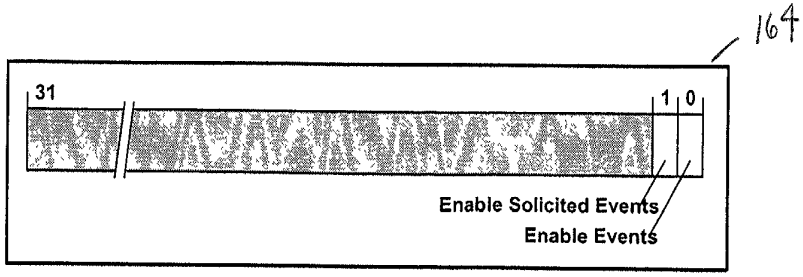

FIG. 12

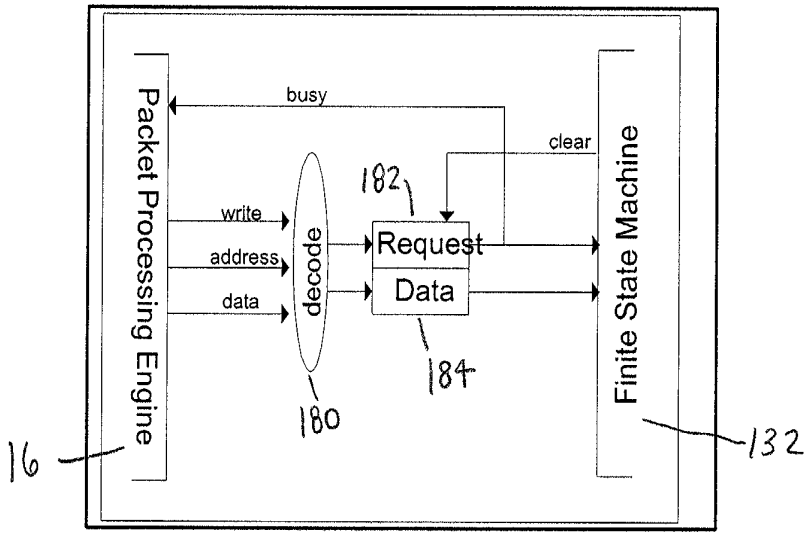

FIG. 13

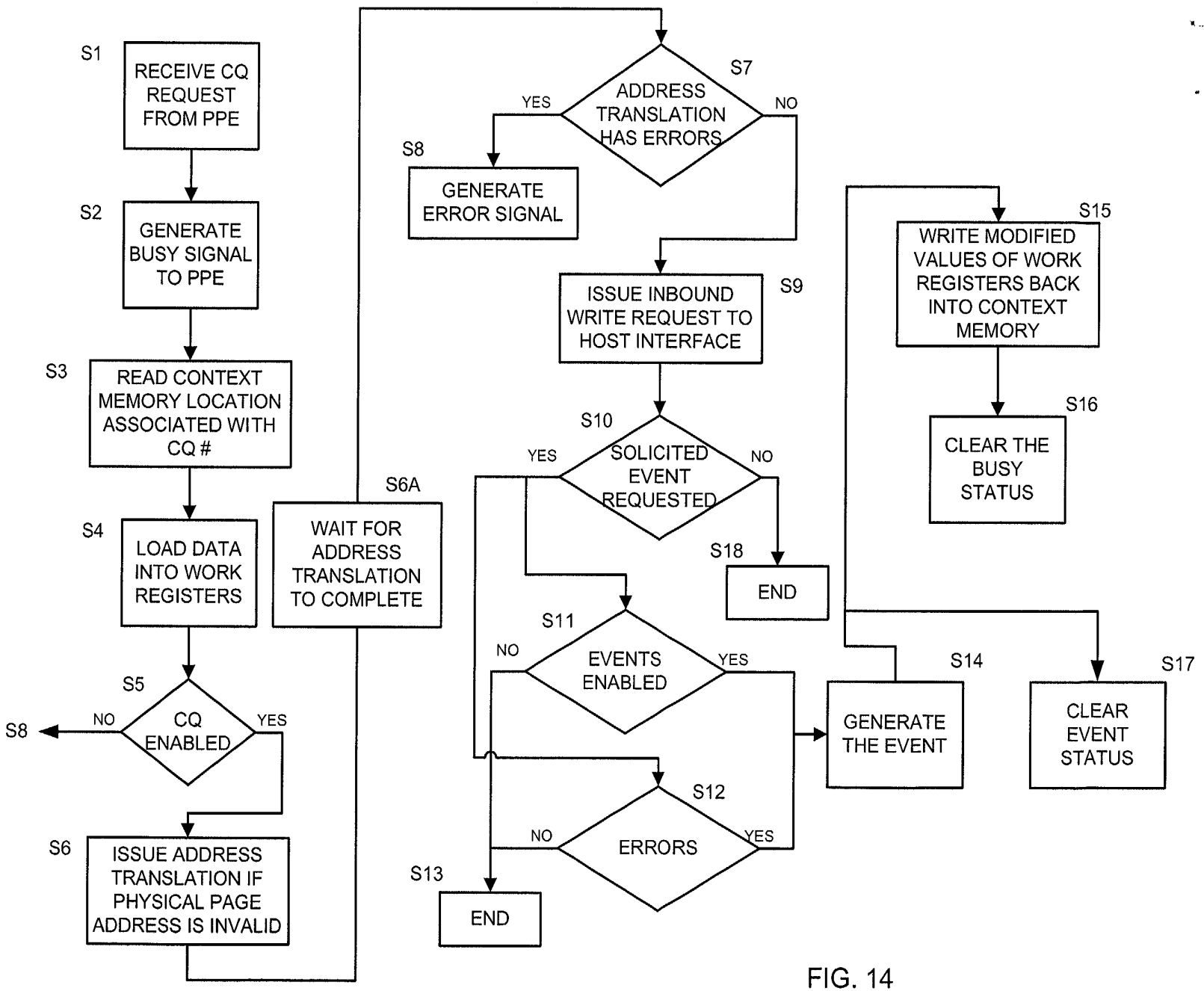
S1
RECEIVE CQ REQUEST FROM PPE
S2
GENERATE BUSY SIGNAL TO PPE
S3
READ CONTEXT MEMORY LOCATION ASSOCIATED WITH CQ #
S4
LOAD DATA INTO WORK REGISTERS
S5
CQ ENABLED
NO
YES
S8
S6
ISSUE ADDRESS TRANSLATION IF PHYSICAL PAGE ADDRESS IS INVALID
S6A
WAIT FOR ADDRESS TRANSLATION TO COMPLETE
S7
ADDRESS TRANSLATION HAS ERRORS
YES
NO
S8
GENERATE ERROR SIGNAL
S9
ISSUE INBOUND WRITE REQUEST TO HOST INTERFACE
S10
SOLICITED EVENT REQUESTED
YES
NO
S18
END
S11
EVENTS ENABLED
NO
YES
S12
ERRORS
NO
YES
S13
END
S14
GENERATE THE EVENT
S15
WRITE MODIFIED VALUES OF WORK REGISTERS BACK INTO CONTEXT MEMORY
S16
CLEAR THE BUSY STATUS
S17
CLEAR EVENT STATUS

FIG. 14

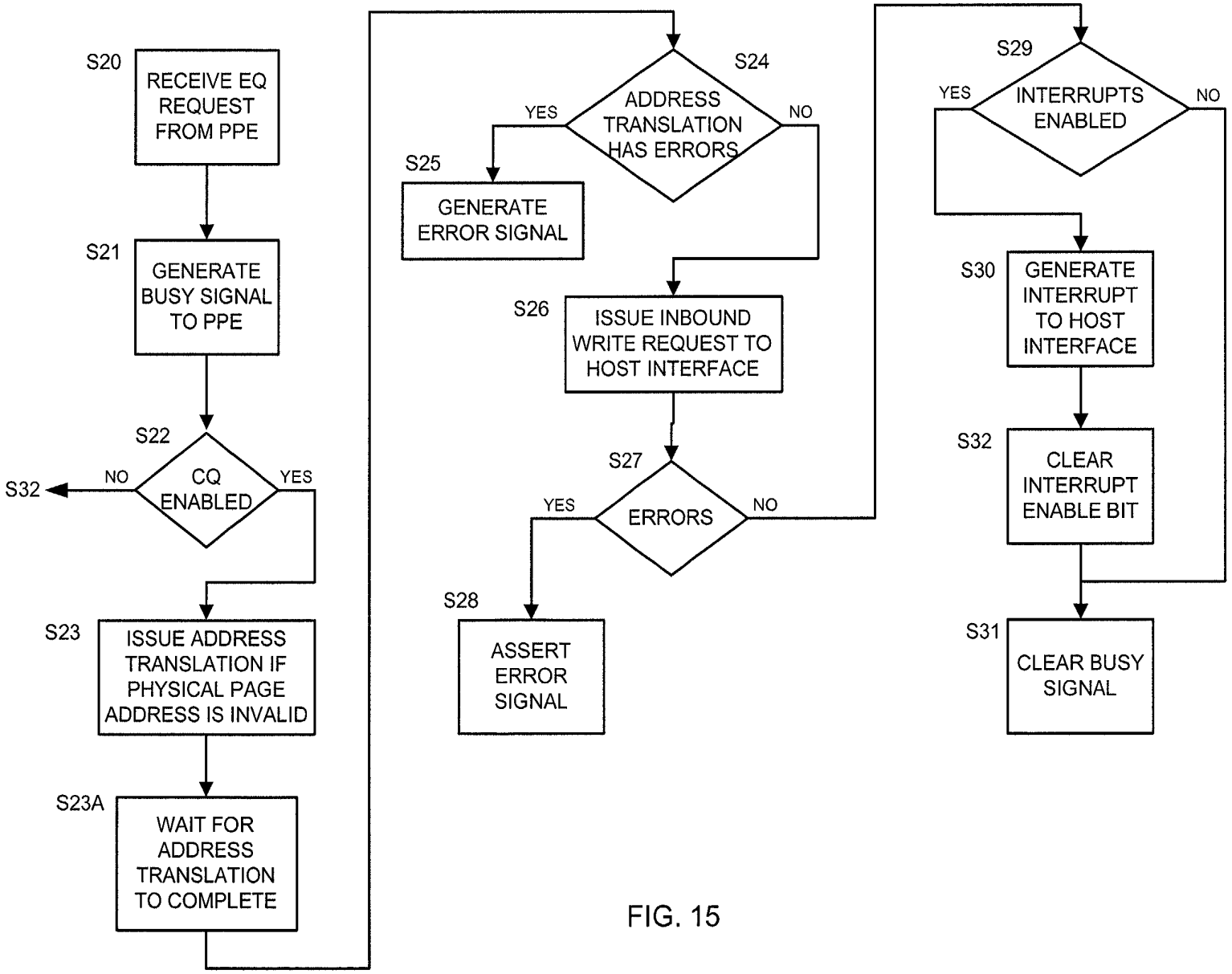
S20
RECEIVE EQ REQUEST FROM PPE
S21
GENERATE BUSY SIGNAL TO PPE
S22
CQ ENABLED
NO
YES
S32
S23
ISSUE ADDRESS TRANSLATION IF PHYSICAL PAGE ADDRESS IS INVALID
S23A
WAIT FOR ADDRESS TRANSLATION TO COMPLETE
S24
ADDRESS TRANSLATION HAS ERRORS
YES
NO
S25
GENERATE ERROR SIGNAL
S26
ISSUE INBOUND WRITE REQUEST TO HOST INTERFACE
S27
ERRORS
YES
NO
S28
ASSERT ERROR SIGNAL
S29
INTERRUPTS ENABLED
YES
NO
S30
GENERATE INTERRUPT TO HOST INTERFACE
S32
CLEAR INTERRUPT ENABLE BIT
S31
CLEAR BUSY SIGNAL

FIG. 15

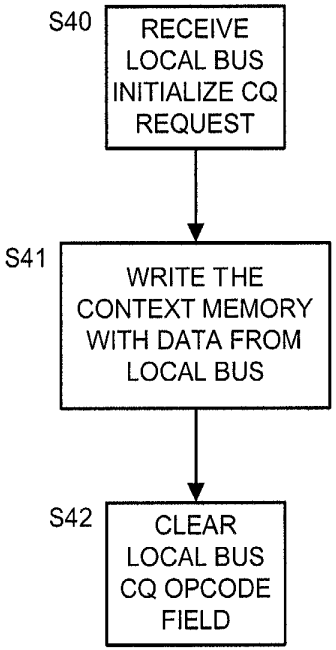

FIG. 16

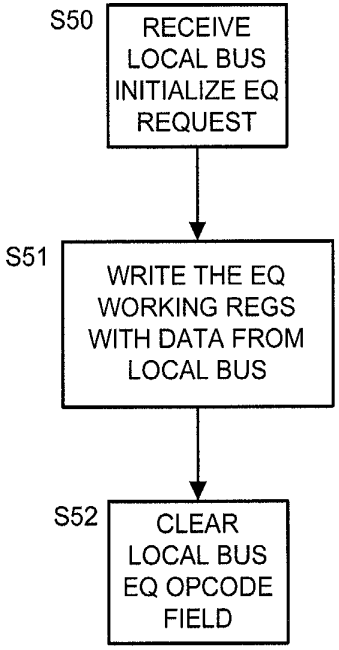

FIG. 17

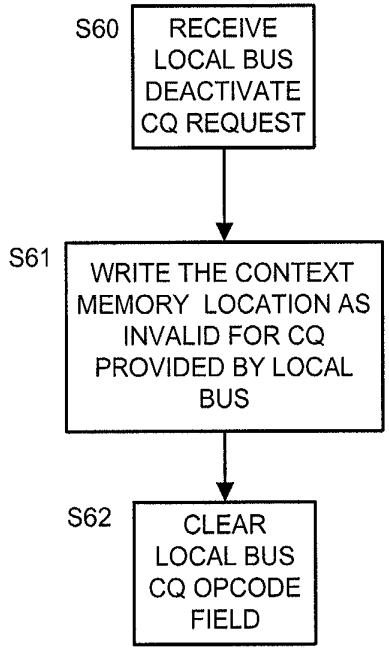

FIG. 18

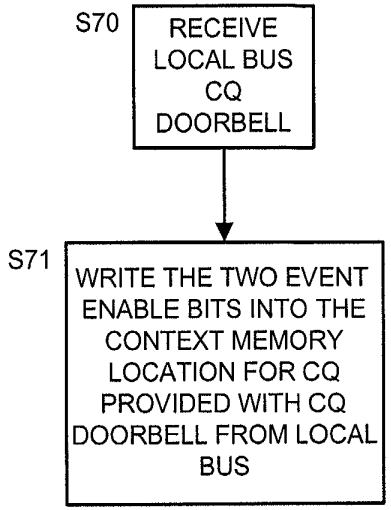

FIG. 19

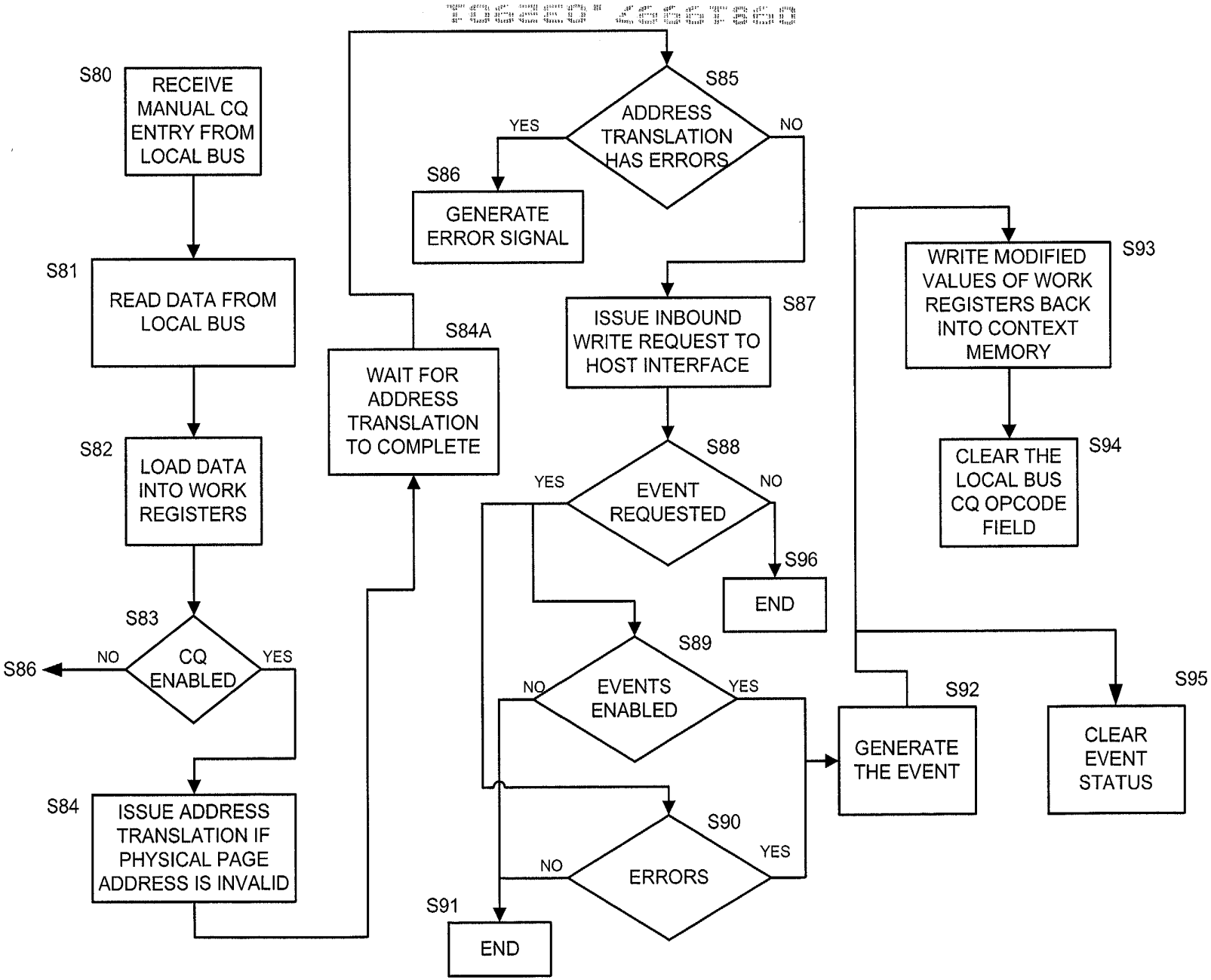
S80
RECEIVE MANUAL CQ ENTRY FROM LOCAL BUS
S81
READ DATA FROM LOCAL BUS
S82
LOAD DATA INTO WORK REGISTERS
S83
CQ ENABLED
NO
YES
S86
S84
ISSUE ADDRESS TRANSLATION IF PHYSICAL PAGE ADDRESS IS INVALID
S84A
WAIT FOR ADDRESS TRANSLATION TO COMPLETE
S85
ADDRESS TRANSLATION HAS ERRORS
YES
NO
S86
GENERATE ERROR SIGNAL
S87
ISSUE INBOUND WRITE REQUEST TO HOST INTERFACE
S88
EVENT REQUESTED
YES
NO
S96
END
S89
EVENTS ENABLED
NO
YES
S90
ERRORS
NO
YES
S91
END
S92
GENERATE THE EVENT
S93
WRITE MODIFIED VALUES OF WORK REGISTERS BACK INTO CONTEXT MEMORY
S94
CLEAR THE LOCAL BUS CQ OPCODE FIELD
S95
CLEAR EVENT STATUS

FIG. 20